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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 09/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,166	PALTASHEV ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-7 and 15-27* is/are withdrawn from consideration.

5)☒ Claim(s) *36 and 37* is/are allowed.

6)☒ Claim(s) *8-14 and 28-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The reply filed on June 7, 2006 has been fully considered in preparing for this Office Action.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 8-14, and 31-35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent Application No. 10/850940. Although the conflicting claims are not identical, they are not patentably distinct from each other because the features of claims 8-14, and 31-35 of the application are contained in claims 1-18 of U.S. Patent Application No. 10/850940.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 31-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Sijistermans (U.S. Patent No. 6,438,676).

Referring to claims 31-33, Sijistermans teaches a data processor that has a compression instruction which refers to two storage units, such as two operand registers, a first register containing one or more codes that specify relative amounts of shift that have to be applied to respective numbers in the second operand register. The relative amounts correspond for example to the lengths of bits to which respective numbers in a second operand register must be

compressed (col. 1, lines 60-67, and col. 2, line 1). As shown in Fig. 5, Sijistermans further teaches a control logic for controlling data select input signals such that individual bits of the plurality of bits are shifted varying amounts, the shift amount being determined by a mask (col. 8, lines 8-14, and 27-65). As shown in Figs. 4, Sijistermans teaches some of the bits are removed (in field 48a) so that the shifted data 47a-47d can overwrite the positions that are to be removed. The control for selecting each individual input of each multiplexer is described on column 10, lines 3-12.

In regard to claim 34, Sijistermans teaches the position of a shifted part 47a-d in the register depends on the sum of the variable lengths of the fields that precede it (col. 4, lines 1-19).

In regard to claim 35, as cited above, since Sijistermans teaches the shift amount is determined by a mask, and the shift amount is variable, the arranged order of the positions of the mask is therefore arbitrary.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8-10, 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sijistermans (U.S. Patent No. 6,438,676) in view of Mahurin (U.S. Patent No. 6,006,244).

Referring to claims 8, 9, 28, and 29, as cited above, Sijistermans teaches a data processor that has a compression instruction which refers to two storage units, such as two operand registers, a first register containing one or more codes that specify relative amount(s) of shift that have to be applied to respective numbers in the second operand register. The relative amount(s) correspond for example to the lengths of bits to which respective numbers in a second operand register must be compressed (col. 1, lines 60-67, and col. 2, line 1). As shown in Fig. 5, Sijistermans further teaches a control logic for controlling data select input signals for the plurality of multiplexers such that individual bits of the plurality of bits are shifted varying amounts, the shift amount being determined by a mask (col. 8, lines 8-14, and 27-65). Sijitermans also teaches that the function unit can be implemented using multiplexers (col. 10, lines 3-12). As shown in Figs. 4, Sijistermans teaches some of the bits are removed (in field 48a) so that the shifted data 47a-47d can overwrite the positions that are to be removed.

Thus, Sijistermans teaches all the limitations of claims 8, 9, 28, and 29, except that the multiplexers arranged in a plurality of rows, wherein multiplexers in a first row have inputs connected to signals defining bits to be compressed and multiplexers of successive rows have inputs connected to outputs of the multiplexers of the preceding row, wherein each successive row of multiplexers comprises fewer multiplexers than the previous row.

However, Mahurin teaches a circuit for shifting or rotating operands of multiple size, wherein as shown in Fig. 2, comprising a plurality of rows of multiplexers, wherein multiplexers in a first row have inputs connected to signals defining bits to be compressed and multiplexers of successive rows have inputs connected to outputs of the multiplexers of the

preceding row, wherein each successive row of multiplexers comprises fewer multiplexers than the previous row.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Mahurin in combination with the method as taught by Sijistermans in order to eliminate the multiple stage pre-shifter and reduce signal propagation delay (col. 4, lines 54-61).

In regard to claims 10 and 30, with reference again to Figs. 4, Sijistermans teaches the control logic to shift individual bits by an amount equal to a number of bit positions, preceding the current bit position, that are to be unaffected by the computation (col. 4, lines 1-19).

7. Claims 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sijistermans (U.S. Patent No. 6,438,676) in view of Mahurin (U.S. Patent No. 6,006,244), further in view of Lumelsky (U.S. Patent No. 5,430464).

Referring to claims 11, 13, and 14, as cited above, Sijistermans and Mahurin teach all the limitations of claims 11, 13, and 14, except that the pixel mask corresponding to a tile of pixels, and the groups of bits defining data values representing an attribute, wherein the attribute is one selected from R, G, B, A, U, and V.

However, Lumelsky teach an image buffer stores compressed image pixel data for a plurality of n x m matrices of pixels, each matrix represented by a pair of color codes and MASK having nm bit position, each positions mapping to a pixel in the matrix, a manifested bit value in a MASK bit position defining the color code assigned to a mapped pixel. The image buffer includes serial registers for feeding pixel color code values to a buffer serial output and multiplexers for providing n bit values from the MASK on n of its output lines (col., lines). As

shown in Fig. 5, the pixel mask is corresponding to a tile of pixels, and the group of bits representing attributes selected from the color (Fig. 5, col. 4, lines 60-68, and col. 5, lines 1-5).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Lumelsky in combination with the method as taught by Sijistermans and Mahurin in order to provide an improved compressed image frame buffer which exhibits a high efficiency in the decompression of the compressed image code (col. 3, lines 50-53).

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sijistermans (U.S. Patent No. 6,438,676) in view of Mahurin (U.S. Patent No. 6,006,244), further in view of Morein et al. (U.S. Patent No. 6,636,226).

Referring to claims 11 and 12, as cited above, Sijistermans and Mahurin teach all the limitations of claims 11and 12, except that the pixel mask corresponding to a tile of pixels, and the pixel mask are based on depth information.

However, Morein et al. teach a method for controlling, or managing, compressed Z information in a video graphics system utilizing a Z-mask information of a pixel block as shown in Fig. 5, and col. 7, lines 62-67, and col. 8, lines 1-47.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Morein et al. in combination with the method as taught by Sijistermans and Mahurin in order to reduce the memory bandwidth requirements in a 3D video graphics system (col. 2, lines 42-45).

Response to Arguments

9. Applicant's arguments filed June 7, 2006 have been fully considered but they are not persuasive.

Double-Patenting Rejection. In response to Applicant's arguments about the double-patenting rejection, since no such restrictions have been made, the rejection is maintained.

Prior Art Rejection. In response to Applicant's arguments that the cited references does not teach "control logic for controlling data select input signals for individual select inputs of the plurality of multiplexers..., and the individual select inputs being determined by a mask," the examiner respectfully disagrees. As cited in previous Office Action and incorporated herein below, Sijistermans teaches a control logic for controlling data select input signals such that individual bits of the plurality of bits are shifted varying amounts, the shift amount being determined by a mask (col. 8, lines 8-14, and 27-65), and the control for each individual input of each multiplexer is described on column 10, lines 3-12.

In response to Applicant's argument that the cited references fail to teach some of input signals are to be removed during compression, and also fail to teach "control logic... to be removed," the examiner again disagrees because this feature is also taught in Sijistermans. With reference, for example to Fig. 4A, Sijistermans teach some of the input signals are to be removed during compression (i.e. portion of the uncompressed data field 44a) are to be removed such that input signals following input signals that are to be removed (such as 46b) are shifted into the position of the preceding signals that are to be removed. The mask defining positions of the plurality of signals is cited above. Since Sijistermans teach the control logic which can be implemented using plurality of multiplexers for selecting input signals into the multiplexers, Mahurin teach the

plurality of multiplexers arranged in a plurality of rows, capable to shift input signals by a number of bits, the combination of the references is therefore proper.

Applicant's arguments also pointed out that the cited reference does not teach "a pixel mask ... associated with pixels to be displayed." In response, the examiner disagrees. In fact, Sijistermans teach processing data and compiling a program for a data processor for use in a computer in its generalized sense, and thus can be applied in processing instructions for pixel data. Applicant's argument also recites the cited reference does not teach "the shift amount for a group of bits is defined by a summation of preceding mask positions... **not to be affected by a subsequence computation**..." the examiner again disagrees. With reference again to Fig. 4, Sijistermans teaches "By "concatenation" of two shifted parts 47a-d is meant that the bits of one shifted part 47a-d follow the bits of another shifted part 47a-d each time at a distance of a predetermined number of bits (preferably directly, at a distance of zero bits), **so that the position of a shifted part 47a-d in the register depends on the sum of the variable lengths of the fields that precede it**.... In principle, only the content of the parts 46a-d appears in the compressed data 42; the remainder of the fields 44a-d of the uncompressed data format 40 does not appear in the compressed data format 42" (col. 4, lines 10-26). Thus, the shift amount determined by the mask as cited above, is the summation of the remainder of the fields 44a-d of the uncompressed format 40, and these remainders of the uncompressed data are unaffected by **subsequent computation.**

Since the cited references meets the minimum requirement of the claims, the rejection is maintained.

Allowable Subject Matter

10. Claims 36-37 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art made of record fails to anticipate or make obvious the claimed invention. Specifically, the prior art fails to teach or suggest the claimed configuration of the multiplexers.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen

8/31/2006

KEE M. TUNG
SUPERVISORY PATENT EXAMINER